Near Sensor Processing Algorithms for Parallel Ultra Low power Architectures

RESEARCH PROJECT

The progress of embedded systems in terms of miniaturization and performance has resulted in a growing push towards their integration in everyday environment and their use in applications such as systems for monitoring buildings and critical infrastructure, but also medical devices for personalized medicine as well as unobtrusive consumer wearables.

Collectively referred to as the end-nodes of the Internet of Things (IoT), these smart and connected devices share the need for extreme energy-efficiency for operation with a power budget of milliwatts. From a system-level perspective, in architectures targeting such applications, the data acquisition is implemented by a sensing subsystem, realized with low-power sensors, such as accelerometers, gyroscopes, microphones, electrical sensors, coupled with low-power analog front-end and analog-to-digital converter. Making sense of data coming from such sensors can be a computationally-intensive task, hence in most approaches information is sent to a computational gateway through a wireless communication subsystem consisting of low-energy TX/RX radio transceivers implementing low-energy stacks.

Despite optimization strategies and advances in low power transceivers design, the overall power budget of these systems is dominated by wireless communication. Hence, a high-potential approach to reduce system energy is to increase the capabilities of near-sensor data analysis and filtering by providing more computational power to the processing sub-system. This approach can dramatically reduce the amount of wireless data transmitted, by shrinking it to a class, a signature, or even just a simple event.

The recent advances in the design of low-power digital architectures, coupled with low-power devices and circuits, is making it possible to perform practical near-sensor computing, especially by leveraging parallel processing. The development of near-sensor processing through the efficient parallelization of algorithms is a key enabling technology and will play a key role in the IoT revolution.

The activity planned will focus on the development of parallelized algorithms tailored for low power near-sensor computing platforms. In particular, we will develop techniques to reduce memory footprint to as to be able to execute complex sensor data processing and classification algorithms on microcontroller-class devices (such as STMicroelectronics STM32).

The focus will be on techniques for data reduction such as principal-component analysis, which can extract the most relevant information from complex, multidimensional signals. The goal will be to demonstrate that these algorithms, which are traditionally executed on powerful computing platforms can “squeezed” to run on a resource-constrained platform as an MCU and that the resulting data reduction leads to an overall boost in energy efficiency thanks to the more parsimonious use of the wireless communication links.
ACTIVITY PLAN

The main training milestones of the activity plan are:
• Development, knowledge and study of techniques and algorithms to increase the intelligence of sensors and actuators both wearable and environmental and increase their energy efficiency.
• Experience in systems design, e.g. for heterogeneous sensors and actuators in closed-loop, based on algorithmic and energy optimization.
• Study of energy efficiency techniques for embedded systems, with special emphasis on STmicroelectronics STM32 platforms.
• Research on signal processing models and compression sampling methods, optimized for resource-constrained low power architectures
• Development of techniques for sensor fusion between different sensors.

The applicative aspects of the training will be on the design and deployment of 2 demonstrators, bearing in mind the trade-off between the use of computational resources, power consumption and the need to communicate with other systems belonging to an intelligent environment.

Steps of the research work:

1. Study of the architecture for an ultra-low power system.

2. Study of techniques to increase the energy efficiency of an IoT node both at hardware level, at system-level through application of power management techniques and at the functional level using domain knowledge.

3. Experiencing on typical instruments (IDEs, SDK, CAD, etc.) for embedded system programming and hardware design for the implementation of intelligent systems, enhanced with sensors and actuators and able to communicate with the environment (eg. Using a gateway) and provide context information.

4. Study of optimization techniques and algorithms for complex platforms with low computational resources and possible commercial outcome

5. Hardware and software design for low-power systems and low supply voltage